LATCH STRUCTURE FOR INTERLOCKED PIPELINED CMOS (IPCMOS) CIRCUITS

ABSTRACT OF THE DISCLOSURE

Circuits and methods for operating a latch structure are disclosed. The circuits include a plurality of stages, and each stage includes a first logic circuit, a latch coupled to a second logic circuit of an adjacent stage and a switch which connects the first logic circuit to the latch in a first state and disconnects the logic circuit from the latch in a second state. A local clock circuit controls the first and second states by providing a locally generated clock signal to activate the switch. The locally generated clock signals are generated by interlocking handshake signals from a local clock circuit of an adjacent stage.